**®**

**Présentation du micro-ordinateur (Partie 1)**

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  | |  | |  | | --- | |  | | |  | |  | |  |  |  | |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 2 | A | | 3 | B | |  | C | | programme |
|  |  |
|  | variables |

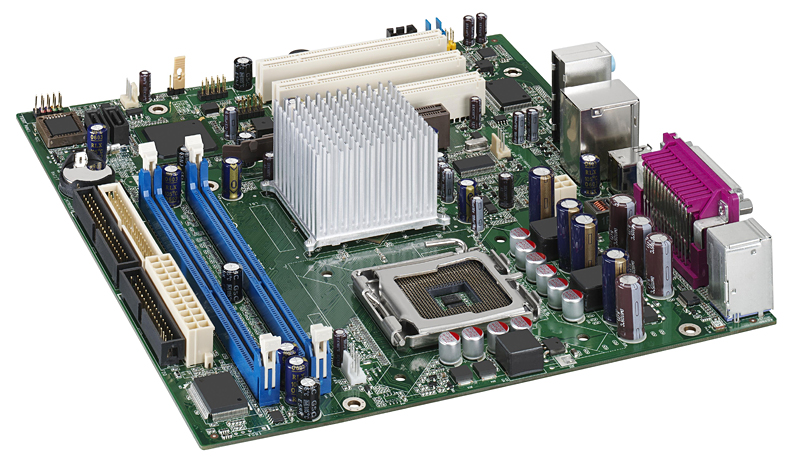
Unités d’entrée

Mémoire de masse

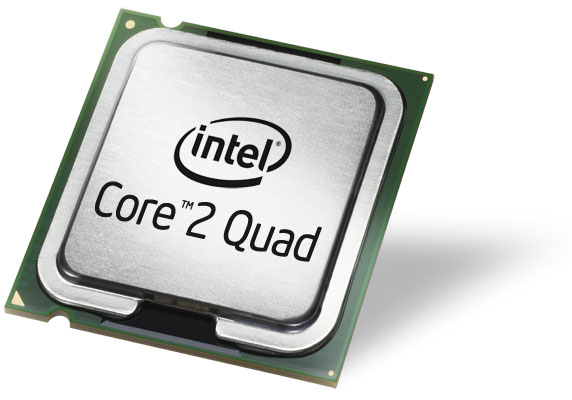
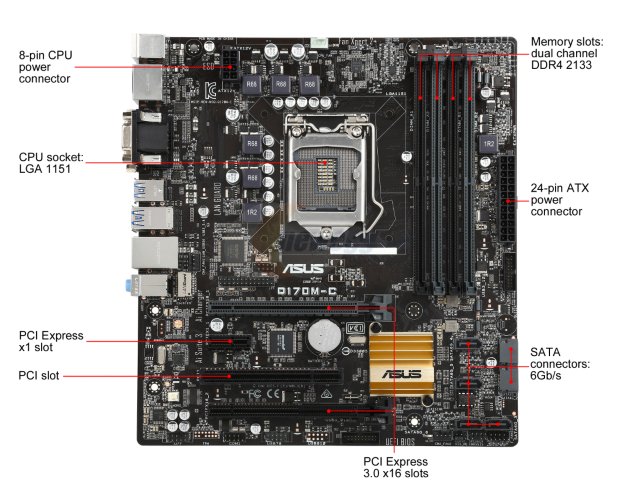
Unités de sortie

Composant secondaire Composant principal

du chipset du chipset (recouvert d’un dissipateur de chaleur)



Connecteurs de mémoire pour barrettes DIMM (en bleu)



Le CPU

Composante principale du micro-ordinateur. (On dira aussi processeur ou micro-processeur).

C’est la composante la plus rapide.

Tâches  effectuées par le CPU : exécute les instructions des programmes et gère les communications avec ses périphériques.

1.Exécute les instructions des programmes

À remarquer : le lien important : CPU-RAM

Notes : --pour raison de commodité : pour les premiers exemples, le contenu de la RAM ne sera pas écrit en binaire comme c’est en réalité, mais en base 16

--RAM : 1 case=1 octet

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  |  |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  | |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | |  | C | | programme |
|  |  |
|  | variables |

Registres : cases mémoire à l’intérieur du CPU

UAL : Unité arithmétique et logique (pour les calculs)

Unité de contrôle : composante qui dirige les opérations à l’intérieur du CPU

Exécution d’uneinstruction :

Étape 1 : L’unité de contrôle demande à la RAM de lui envoyer la prochaine instruction qui doit être exécutée (ici : C+A+B). L’instruction est placée dans un des registres du CPU.

Note : c’est une copie de l’instruction qui est envoyée au CPU.

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  |  |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |   Unité de contrôle |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | | 05 | C | | programme |
| Transférer dans le CPU la prochaine instruction à exécuter |  |
|  | variables |

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |   Unité de contrôle | C+A+B | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | |  | C | | programme |
|  |  |
|  | variables |

Étape 2 : L’unité de contrôle demande ensuite à la RAM de lui envoyer le contenu des variables A et B. Ces contenus sont aussi placés dans des registres du CPU (une copie aussi, comme pour les instructions).

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |   Unité de contrôle |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | | 05 | C | | programme |
| Transférer dans le CPU le contenu de la variable A |  |
|  | variables |

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |   Unité de contrôle | 02 | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | |  | C | | programme |
|  |  |
|  | variables |

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |   Unité de contrôle |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | | 05 | C | | programme |
| Transférer dans le CPU le contenu de la variable B |  |
|  | variables |

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | |  | | |  | 03 | |  |  | |  |  |  |   Unité de contrôle | 03 | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | |  | C | | programme |
|  |  |
|  | variables |

Étape 3 : Le CPU a maintenant tout ce qu’il faut pour exécuter l’instruction. L’unité de contrôle commande à l’UAL de faire l’opération arithmétique.

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| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | | 02+03  05 | | |  | 03 | |  |  | |  |  |  |   Unité de contrôle |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | |  | C | | programme |
|  |  |
|  | variables |

Étape 4 : Le résultat de l’opération arithmétique est placé dans un autre registre du CPU.

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | | 02+03  05 | | |  | 03 | |  | 05 | |  |  |  |   Unité de contrôle |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | |  | C | | programme |
|  |  |
|  | variables |

Étape 5 : L’unité de contrôle demande à la RAM de placer le résultat dans la variable C

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | registres |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | | 02+03  05 | | |  | 03 | |  | 05 | |  |  |  |   Unité de contrôle |  | |  |  | | --- | --- | |  |  | | . . . |  | | C=A+B |  | | . . . |  | |  |  | | 02 | A | | 03 | B | | 05 | C | | programme |
| Transférer dans la RAM la valeur 05 dans la variable C |  |
|  | variables |

L’unité de contrôle demande ensuite à la RAM de lui envoyer l’instruction suivante.

**Notion d’adresses en RAM**

Jusqu’à présent, nous avons utilisé des noms de variables pour identifier les cases mémoires qui contiennent les données et les résultats. En fait, pendant l’exécution du programme, ce sont des adresses qui sont utilisées. Chaque case mémoire (donc octet) est numéroté. On appelle ces numéros des adresses.

Les noms de variables sont pour le programmeur et les adresses sont utilisées par l’ordinateur. Avant l’exécution d’un programme, il y a une correspondance qui est faite entre les variables et les adresses en RAM. Cette opération est transparente à l’usager.

Reprenons l’exemple vu précédemment : (le programme a été placé en RAM par le système d’exploitation)

Si A est associé à l’adresse 0068, B à l’adresse 0069, C à l’adresse 006A on aura en RAM :

|  |  |  |
| --- | --- | --- |
| Adresses  (16 bits) | Contenu  (8 bits) |  |
|  | . . . |  |
| 0025 | C=A+B | Instruction C=A+B du progr |
|  | . . . |  |
|  |  |  |
| 0068 | 02 | A |
| 0069 | 03 | B |
| 006A | 05 | C |
|  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  |  |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 02 | | 0069 | 03 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A | programme  variables |
|  |
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L’étape 2 de la page 3 était :

Étape 2 : L’unité de contrôle demande ensuite à la RAM de lui envoyer le contenu des variables A et B. Ces contenus sont aussi placés dans des registres du CPU (une copie aussi, comme pour les instructions).

Elle devient :

Étape 2 : L’unité de contrôle demande ensuite à la RAM de lui envoyer le contenu des ADRESSES 0068 et 0069. Ces contenus sont aussi placés dans des registres du CPU (une copie aussi, comme pour les instructions).

|  |  |  |  |
| --- | --- | --- | --- |
| CPU |  | RAM |  |
| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 02 | | 0069 | 03 | | 006A |  | | programme  variables |
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**Notion de bus**

Les informations qui circulent entre le CPU et la RAm sont de 3 types : commandes du CPU à la RAM, adresses et contenu de la RAM (revoir l’exécution d’une instruction pages 3 à 5).

Il existe des voies de communication entre toutes les composantes de l’ordinateur. Ce sont les bus. Dans les exemples précédents, j’ai utilisé une seule ligne pour représenter toutes les voies de communication. En fait, il en existe 3 : bus de contrôle, bus d’adresses et bus de données , selon les informations qui y circulent.

Le bus de contrôle sert entre autres à véhiculer les commandes du CPU (ici vers la RAM)

Le bus d’adresses sert à véhiculer les adresses (ici, les adresses de la RAM)

Le bus de données sert à véhiculer les contenus associés aux adresses (ici, le contenu de la RAM)

Si on indique les 3 types de bus, lien entre le CPU et la RAM devient :

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  |  |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Bus de contrôle | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 02 | | 0069 | 03 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A | programme  variables |
| Bus d’adresses |
| Bus de données |
|  |
|  |
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Reprenons l’exemple des pages 3 et 4 avec les 3 types de bus :

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) |  |   Étape 2 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 0068 (bus de contrôle –orange et bus d’adresses – vert). | programme  variables |
| Le contenu de 0068 🡪 |
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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) |  |   Étape 2 : La RAM envoie la valeur demandée (02) via le bus de données (bleu). | programme  variables |
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| 🡨 02 |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) |  |   Étape 2 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 0069 (bus de contrôle –orange et bus d’adresses – vert). | programme  variables |
| Le contenu de 0069 🡪 |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) |  |   Étape 2 : La RAM envoie la valeur demandée (03) via le bus de données (bleu). | programme  variables |
|  |
| 🡨 03 |
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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | | 02+03  = 05 | | |  | 03 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) |  |   Étape 3 : L’unité de contrôle demande à l’UAL de faire l’addition | programme  variables |
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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | |  | | |  | 03 | |  | 05 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) |  |   Étape 4 : Le résultat de l’addition est placé dans un registre du CPU | programme  variables |
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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 02 | |  | | --- | |  | | |  | 03 | |  | 05 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds la RAM 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) |  |   Étape 5 : L’unité de contrôle demande à la RAM de placer le résultat à l’adresse 006A  Remarque : un transfert vers la RAM se fait en une fois, tandis qu’un transfert vers le CPU prend 2 fois. | programme  variables |
| À l’adresse 006A 🡪 |
| 05 🡪 |
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Résultat, l’instruction est exécutée :

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| |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 (A) | 02 | | 0069 (B) | 03 | | 006A (C) | 05 | | programme  variables |

En binaire maintenant :

Un bus est un ensemble de fils de cuivre (1 bit par fil). Un bus de 8 bits a donc 8 fils.

Pour notre exemple :

Le bus d’adresses (bus vert) sert à transporter des adresses de 16 bits. Il aura donc 16 fils.

Le bus de données (bus bleu) sert à transporter des octets. Il aura donc 8 bits.

Nous ne parlerons pas du bus de contrôle (ou très peu…)

Si on complète le schéma de la page précédente avec les bus détaillés, on a :

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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A | variables |
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L’exemple de l’exécution de l’instruction C=A=B devient : (à partir de l’étape 2)

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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Étape 2 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 0068 (bus de contrôle –orange et bus d’adresses – vert).  Comparer avec page 9 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Étape 2 : La RAM envoie la valeur demandée (02) via le bus de données (bleu).  Comparer avec la page 9 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 00000010 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Étape 2 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 0069 (bus de contrôle –orange et bus d’adresses – vert).  Comparer avec la page 10 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 00000010 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Étape 2 : La RAM envoie la valeur demandée (03) via le bus de données (bleu).  Comparer avec la page 10 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  |  | |  | 00000010 | |  | | --- | |  | | |  | 00000011 | |  |  | |  | UAL |  | | 00000010  00000011  00000101 |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Étape 3 : L’unité de contrôle demande à l’UAL de faire l’addition | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 00000010 | |  | | --- | |  | | |  | 00000011 | |  | 00000101 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Étape 4 : Le résultat de l’addition est placé dans un registre du CPU | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 00000010 | |  | | --- | |  | | |  | 00000011 | |  | 00000101 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds la RAM 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A |  |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Étape 5 : L’unité de contrôle demande à la RAM de placer le résultat à l’adresse 006A  Comparer avec la page 12 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | C=A+B |  | |  |  | UAL | |  | 00000010 | |  | | --- | |  | | |  | 00000011 | |  | 00000101 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 0025 | C=A+B | |  |  | | 0068 | 00000010 | | 0069 | 00000011 | | 006A | 00000101 |   A est à l’adresse 0068  B est à l’adresse 0069  C est à l’adresse 006A  Résultat 00000101 (5) dans la variable C (adresse 006A) | variables |
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Exercice : écrire ce qui se passe lors des étapes de l’exécution de l’instruction suivante : S = N1+N2+N3

Cette instruction est placée en RAM à l’adresse 1A00.

Les variables N1,N2,N3 et S prennent chacun 1 octet signé et sont placées en RAM respectivement aux adresses 1A61,1A62,1A63 ert 1A64.

Les valeurs lues pour N1,N2 et N3 sont respectivement : 1210,-2210 et 610

Commencer à partir de l’étape 2, une fois que l’instruction est dans le CPU.

Faire des copies du gabarit de la page suivante tant que nécessaire…

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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64  Unité de contrôle demande à l’UAL de faire l’opération arithmétique (12-22+6)  -4 = 11111100 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  | 11111100 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  | 11111100 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  | 11111100 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S = N1+N2+N3 | |  |  | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 | 11111100 |   N1 est à 1A61 N2 est à 1A62  N3 est à 1A63  S est à 1A64 | variables |
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**Solution**

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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 2 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 1A61 (bus de contrôle (orange) et bus d’adresses (vert)) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  |  | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 2 : La RAM envoie la valeur demandée via le bus de données (bleu) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 2 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 1A62 (bus de contrôle (orange) et bus d’adresses (vert)) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  |  | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 2 : : La RAM envoie la valeur demandée via le bus de données (bleu) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds le CPU 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 2 : L’unité de contrôle demande à la RAM de lui envoyer le contenu de l’adresse 1A63 (bus de contrôle (orange) et bus d’adresses (vert)) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  |  | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 2 : La RAM envoie la valeur demandée via le bus de données (bleu) | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  |  | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 3 : L’unité de contrôle demande à l’UAL de faire l’opération arithmétique (12-22+6)  Résultat : -4 = 11111100 en représentation interne | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  | 11111100 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | bbb | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 4 : Le résultat de l’opération arithmétique (11111100) est placé dans un registre du CPU | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  | 11111100 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | | Transférer ds la RAM 🡪 | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 |  |   Étape 5 : L’unité de contrôle demande à la RAM de placer le résultat à l’adresse 1A64 | variables |
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| |  |  |  | | --- | --- | --- | |  | Registres  (8 bits) |  | |  | S=N1+N2+N3 |  | |  | 00001100 | UAL | |  | 11101010 | |  | | --- | |  | | |  | 00000110 | |  | 11111100 | |  |  |  |  |  |  |  | | --- | --- | --- | |  |  |  | |  | Unité de contrôle |  | |  | |  |  | | --- | --- | |  |  | | **Adresses**  **16 bits** | **Contenu**  **8 bits** | |  | … | | 1A00 | S=N1+N2+N3 | |  | … | | 1A61 | 00001100 | | 1A62 | 11101010 | | 1A63 | 00000110 | | 1A64 | 11111100 |   Résultat : 11111100 (-4) dans la variable S (adresse 1A64) | variables |
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